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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,292	06/30/2003	Seung Cheol Bae	40296-0007	8519

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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,292	BAE, SEUNG CHEOL	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-9* is/are rejected.

7)☒ Claim(s) *2 and 10-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed on 7/2/04 has been received and entered in the case. The amendment presented therein overcomes the previous informality objections, and therefore, are withdrawn. In view of the reconsideration, new grounds of rejections are needed as set forth below. This action is NON-FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4 and 6-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (Foreign Application No. 2000-86612, publication date 4/30/01). US Patent No. 6,552,587 cited in the previous Office action will be used as a translation copy of the cited Foreign Application No. 2000-86612.

As per claim 1, Kim discloses a device (Fig. 6) for controlling a setup/hold time of an input signal, comprising:

a driver (inverter IN1) for outputting a global bus line control signal (the signal labeled "INPUT SIGNAL OF PHASE DETECTOR") by amplifying (inverter has been known for

amplifying an input signal) an output signal (the signal output from the buffer 102) from an input buffer (101 and 102);

a signal delay unit (capacitors Cd and Cd') for delaying the global bus line control signal selectively connected (selected by transmission gates TG1-TG4) to the driver;

a decoding unit (Fig. 5) for outputting a test mode delay signal (control signals Fd1, Fd2, Bd1, Bd2, Kim uses different name, however, using different name does not distinguish the claim from the prior art) by decoding a test control signal (LSRS, as shown in Fig. 5, the signal Fd1 "decoding" the signal LSRS) for determining to control setup/hold time corresponding to the global bus line control signal (determined by setting either LSRS to HIGH or LOW), a test mode entry signal (A1, the signal Fd1 "decoding" the signal A1), and a test mode exit signal (PGM, the signal Fd1 "decoding" the signal PGM); and

a delay control unit (transmission gates TG1-TG4) for controlling the setup/hold time of the global bus line control signal by selectively connecting the signal delay unit to the driver according to a state of the test mode delay signal (controlling the TG1-TG4 to open or close the paths connecting capacitors Cd, Cd' to the first and second nodes).

As per claim 4, Kim further discloses the signal delay unit comprises:

a first capacitor unit (Cd in block 111) connected selectively (by TG1) to a first node (Nod1) of the driver controlled by the delay control unit (TG1); and

a second capacitor unit (Cd' in block 122) connected selectively (by TG4) to a second node (Nod2) of the driver controlled by the delay control unit (TG4).

As per claim 6, Kim further discloses the delay control unit comprises:

a first delay control unit (TG1) for delaying (column 6, line 64, "increasing") the setup/hold time of the global bus line control signal by selectively connecting the first capacitor unit to the first node according to a first state of the test mode delay signal (when Fd1 is HIGH, TG1 is ON, the first capacitor unit Cd in block 111 is connected to the first node Nod1); and

a second delay control unit (TG4) for advancing (column 6, line 65, "decreasing") the setup/hold time of the global bus line control signal by selectively connecting the second capacitor unit to the second node according to a second state of the test mode delay signal (when Bd2 is LOW, TG4 is ON, the second capacitor unit Cd' in block 122 is connected to the second node Nod2).

As per claim 7, the recited first delay control unit reads on transmission gate TG1 which comprises a first transmission gate (transistor NMOS of TG1) and a second transmission gate (transistor PMOS of TG1) as recited.

As per claim 8, the recited second delay control unit reads on transmission gate TG4 which comprises a third transmission gate (transistor NMOS of TG4) and a fourth transmission gate (transistor PMOS of TG4) as recited.

As per claim 9, the Kim's decoder shown in Fig. 5 is clearly able to provide the recited function.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (Foreign Application No. 2000-86612, publication date 4/30/01). US Patent No. 6,552,587 cited in the previous Office action will be used as a translation copy of the Foreign Application No. 2000-86612.

A per claim 3, Kim discloses a device for controlling a setup/hold time of an input signal having a structure discussed in claim 1 wherein the driver comprises an inverter IN1 but he does not explicitly disclose the driver comprises an even number of inverters as called for in the claim.

As known by a person skilled in the art, using an odd number of inverters to implement a driver circuit would generate an inverted delayed output signal of the input signal whereas using an even number of inverters to implement a driver circuit would generate a non-inverted delayed output signal of the input signal.

It would have been obvious to one skilled in the art at the time of the invention was made to add another inverter IN1' to the Kim's driver circuit. The motivation and/or suggestion for doing so would be to generate a non-inverted delayed output signal of the input signal when the Kim's device is used for controlling a setup/hold time of an input signal for applications which require the output signal is a non-inverted delayed of the input signal.

As per claim 5, Kim discloses a device for controlling a setup/hold time of an input signal wherein the first and second capacitor units are capacitors (Cd, Cd') but he does not explicitly disclose the capacitors are MOS capacitors.

The examiner takes Official Notice the fact that using a MOS transistor to implement a capacitor is a well-known practice.

It would have been obvious to one skilled in the art at the time of the invention was made to implement capacitors Cd in the Kim's device using MOS transistors. The motivation would be to minimize the size of the device, i.e., MOS capacitor occupies less real estate than any other conventional capacitors.

Allowable Subject Matter

4. Claims 2 and 10-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 2 is allowable because the prior art of record fails to disclose or suggest the inclusion of a first latch for latching the global bus line control signal.

Claims 10-13 are allowable because the prior art of record fails to disclose or suggest the inclusion of a logic unit, second and third latches in the decoder unit as recited in claim 10.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

9/3/04

Minh Nguyen
Primary Examiner
Art Unit 2816